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L2: Entry 46 of 100 File: USPT Jun 13, 2000

DOCUMENT-IDENTIFIER: US 6074947 A
TITLE: Process for improving uniform thickness of semiconductor substrates using plasma assisted chemical etching

Detailed Description Text (3):
In accordance with the present invention, it has been discovered that both the resulting global flatness as well as the quality of a semiconductor substrate can be improved by selectively removing material from the back surface of a substrate by plasma assisted chemical etching using a mathematically inverted dwell time versus position map. Surprisingly, it has been discovered that because silicon substrates are extremely flexible and freely conform under vacuum to the flat surface of device fabrication chucks, removing material from the unpolished back surface of the substrate is an effective means for improving non-uniformity and global flatness of the substrate without introducing contamination or defects onto the front surface subsequently utilized for device fabrication.

L2: Entry 43 of 100 File: USPT Jul 11, 2000

DOCUMENT-IDENTIFIER: US 6086976 A
TITLE: Semiconductor wafer, handling apparatus, and method

Brief Summary Text (10):
Conventional wafer processing steps are generally performed by resting the backside of the wafer on a flat support surface. In order to process the backside of the wafer, conventional means may require turning the wafer over and resting it on the front side of the wafer. This also involves resting the wafer on its front side which increases the likelihood that contaminates will be introduced to the chips or dies on the front side of the wafer. This involves increased processing steps (turning the wafer over) as well as more direct handling of the wafer. Increased direct handling adds further risk of damaging the chips or dies contained on the wafer from particulates that may become dislodged from such handling.

WEST Search History

DATE: Tuesday, January 28, 2003

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ		
L18	L16 and l3	3	L18
L17	L16 same (chuck$3 or piedestal or hold$3 or support$3)	47	L17
L16	L15 with ((back surface) or (back side) or backside or (second side))	91	L16
L15	(wafer or substrate or semiconductor) with (edge bead) with (clean$3 or remov$3)	251	L15
L14	L13 same (chuck$3 or piedestal or hold$3 or support$3)	1692	L14
L13	L11 same ((back surface) or (back side) or backside or (second side))	7886	L13
L12	L11 and l3	1408	L12
L11	(wafer or substrate or semiconductor) same ((edge bead) with clean$3 or remov$3)	303794	L11
L10	L9 and l3	0	L10
L9	((pre treat$3) or (pre condition$3) or (pre clean)) same ((wafer or substrate or semiconductor) with (back surface) or (back side) or backside or (second side))	40	L9
L8	L7	30	L8
L7	L6 and l3	30	L7
L6	(wafer or substrate or semiconductor) with ((back surface) or (back side) or backside or (second side)) with (clean$3 or remov$3 or planar$5 or uniform$5 or polish$3 or flat$7) with (chuck$3 or piedestal or hold$3 or support$3)	1139	L6
L5	((pre treat$3) or (pre condition$3) or (pre clean)) same (wafer or substrate or semiconductor) same ((back surface) or (back side) or backside or (second side)) same (chuck$3 or piedestal or hold$3 or support$3)	4	L5
L4	L3 and l1	8	L4
L3	((134/902)!.CCLS. |(438/906)!.CCLS.)	2156	L3
L2	(wafer or substrate or semiconductor) with ((back surface) or (back side) or backside or (second side)) adj5 (planar$5 or uniform$5 or flat$7) with (chuck$3 or piedestal or hold$3 or support$3)	100	L2
L1	(wafer or substrate or semiconductor) with ((back surface) or (back side) or backside or (second side)) adj5 (planar$5 or uniform$5 or polish$3 or flat$7) with (chuck$3 or piedestal or hold$3 or support$3)	184	L1

END OF SEARCH HISTORY